CLAIMS

What is claimed is:

1. A method of allocating a trace array from a cache memory, comprising:
dividing said cache memory into a reduced-size cache memory and a trace array;
permitting storage of trace signal data into said trace array; and
permitting retrieval of said trace signal data from said trace array.

2. A method as defined in Claim 1 wherein said reduced-size cache memory is equal in size to said trace array.

3. A method as defined in Claim 1 wherein said reduced-size cache memory is not equal in size to said trace array.

4. A method as defined in Claim 1 wherein said cache memory is 512K bytes in size.

5. A method as defined in Claim 1 wherein at least one of said cache memory and said reduced-size cache memory is organized in eight-way associativities.

6. A method as defined in Claim 1 wherein said cache memory comprises a directory array.

7. A method as defined in Claim 6 wherein said directory array comprises an address field having a spare bit usable in a trace mode to represent a high order bit of a requested address.

8. A method as defined in Claim 1, further comprising:
detecting a trace mode.

9. A method as defined in Claim 1 wherein said cache memory is comprised by a system-on-chip environment.

10. A method as defined in Claim 1 wherein the combination of said reduced-size cache memory and said trace array comprises a split cache spanning the addressable space of said cache memory.

11. A method as defined in Claim 1 wherein the permitted retrieval of said trace signal data from said trace array is configured as a broadside output from said trace array.

12. A method as defined in Claim 1 wherein the permitted retrieval of said trace signal data from said trace array is configured as a compartmentally selected output from said trace array.

13. A method as defined in Claim 1 wherein said reduced-size cache memory and said trace array are each associated with a separate output bus.

14. A method as defined in Claim 1, further comprising:
characterizing a self-timed interconnect using said trace array; and
switching back to the original cache functionality once characterization is complete.

15. A method as defined in Claim 14, further comprising:

at least one of multiplexing and time-sharing said self-timed interconnect signals with other signals to be stored in said trace array.

16. A storage medium encoded with a machine-readable computer program code for allocating a trace array from an original cache memory, said storage medium including instructions for causing a computer to implement a method comprising:

dividing the cache memory into a reduced-size cache memory and a trace array;

permitting storage of trace signal data into said trace array; and

permitting retrieval of said trace signal data from said trace array.

17. A computer data signal for allocating a trace array from an original cache memory, said computer data signal comprising code configured to cause a computer to implement a method comprising:

dividing the cache memory into a reduced-size cache memory and a trace array;

permitting storage of trace signal data into said trace array; and

permitting retrieval of said trace signal data from said trace array.

18. A cache memory comprising:

means for dividing said cache memory into a reduced-size cache memory and a trace array;

means for permitting storage of trace signal data into said trace array; and

means for permitting retrieval of said trace signal data from said trace array.